1 2

3

1

2

3

What is claimed is:

4	4 1' ', 1		•		
	A digital	cional	nrocessing	circilit	comprising
1.	11 digitar	Signar	processing	Ollouit	comprising

- a chain of processing units to receive indications of discrete input values, each processing unit being associated with one of a group of filter coefficients; and
- a tap selection circuit to select a group of the processing units of the chain to produce an indication of a filtered discrete output value for each discrete input value.
- 2. The processing unit of claim 1, wherein the chain of processing units comprises a systolic chain.
 - 3. The processing circuit of claim 1, wherein the tap selection circuit selects a number of taps of the processing circuit.
 - 4. The processing circuit of claim 1, wherein the group of processing units progressively accumulate a summed value to form each output value and the tap selection circuit comprises:
 - a multiplexer to designate a point in the chain at which the accumulation begins.
 - first input terminal to receive the indications of the discrete input values from a processing circuit input line common to the processing circuits and a second input terminal to receive the
- 4 indications of the discrete input values from another processing circuit, the multiplexer coupling
- 5 the first and second terminals of one of the processing circuits together to designate the point in
- 6 the chain at which the accumulation begins.

2

1

2

1	The among singuit of claim 1 wherein each among singuit commission
1	6. The processing circuit of claim 1, wherein each processing circuit comprises:
2	a first adder circuit to generate an indication of a summation of two of the discrete input
3	values; and
4	a multiplier circuit coupled to the first adder circuit to generate an indication of a product
5	of a coefficient associated with said each processing circuit and the summation of the two
6	discrete values.
1	7. The processing circuit of claim 6, further comprising:
2	a second adder circuit coupled to the first multiplier circuit to combine the summation of
3	the two discrete input values with a progressive summation provided by another processing
4	circuit.

- 8. The processing circuit of claim 7, wherein the tap selection circuit comprises: a multiplexer to selectively furnish an indication of a zero to the second adder circuit of one of the processing units to designate a point where the progressive sum begins.
 - 9. The processing circuit of claim 1, wherein the tap selection circuit comprises: a register storing bits indicative of the processing units in the group.
 - 10. The processing circuit of claim 1, wherein each processing unit comprises: a register storing the indication of the associated filter coefficient.
- The processing circuit of claim 1, wherein the processing circuit comprises a finite impulse response filter.
- 12. The processing circuit of claim 1, wherein the processing circuit comprises an infinite impulse response filter.

1	13.	A digital signal processing circuit comprising:		
2	a proc	a processing chain having a selectable number of taps; and		
3	a tap	selection circuit coupled to the processing chain to selectively establish the number		
4	of taps of the	chain.		
1	14.	The processing circuit of claim 13, wherein the tap selection circuit comprises:		
2	a mul	tiplexer to select one of the taps as the beginning tap in the chain.		
1	15.	The processing circuit of claim 14, wherein the multiplexer sets a cumulative sum		
2	at the selected	d tap to zero.		
1	16.	The processing circuit of claim 14, wherein the multiplexer sets a delay at the		
2	selected tap to	o zero.		
1	17.	The processing circuit of claim 13, wherein the tap selection circuit comprises:		
2	a regi	ster storing bits indicative of the number of taps.		
1	18.	The processing circuit of claim 13, wherein the tapped delay line comprises:		
2	regist	ers storing indications of filter coefficients associated with the taps.		
1	19.	The processing circuit of claim 13, wherein the processing circuit comprises a		
2	finite impulse	e response filter.		
1	20.	The processing circuit of claim 13, wherein the processing circuit comprises an		
2	infinite impul	lse response filter.		
1	21.	A method comprising:		
2	provid	providing a processing chain line having a fixed number of taps;		
3	disabl	ing some of the taps of the chain; and		
4	using	the remaining taps to establish a finite impulse response filter.		

1	22. The method of claim 21, wherein the disabling comprises:
2	selecting one of the taps as the beginning tap in the delay line.
1	23. The method of claim 21, wherein the disabling comprises:
2	setting a cumulative sum at one of the taps to zero.
1	24. The method of claim 21, further comprising:
2	storing bits indicative of the number of remaining taps.
1	25. The method of claim 21, further comprising:
2	storing rewritable indications of filter coefficients associated with the taps.